

## ANALYSIS OF FINFET CHARACTERISTICS WITH GATE LENGTH SCALLING

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### Abstract

The effect of gate length variations of a FinFET device (6 x 7 nm width and height) by performing 3D Silvaco TCAD simulations was investigated. In addition, comparative Atomistics ToolKit by QuantumWise simulations were done, with a view to TCAD / ATK functionality at quantum effects. Both systems use Non-Equilibrium Green Functions (NEGF) for electron quantum transport simulation. The ATK tool uses the real atom positions in the device crystal lattice for the Density Functional Theory (DFT) based calculations moreover. It is found that the gate length influences the drain current mostly for small voltages. Short gate transistors show the saturation current for clearly lower voltages, the saturation current for longer gates is achieved for higher voltages but get lower values. Electron transmission functionality of system's energy has been analyzed as well. The ATK uses more precise quantum models, but the time consumption is enormous for the relative large structures as FinFET. 3D TCAD quantum model is sufficient for the faster analysis of quantum semiconductor device.

**Keywords:** FinFET, TCAD, drain current, electron transmission, gate length

### 1 INTRODUCTION

According to integrated circuit development, a whole system tends to be smaller, compacter and faster, each feature size tends to be minimalized. However, as the features have become finer, negative quantum effects appeared. The smaller the features are, the higher the quantum effect impact is. Typically, high leakage current appear because of short-channel effects, nextly, material doping has become non-trivial. In order to refine the transistor sizes, a thin-body double-gate MOSFET structure was proposed by team of UC Berkeley (led by Dr. Chenming Hu). Such a double-gate planar feature would suppress leakage by keeping the gate capacitance closer to the whole of the channel. From this 2D geometry, a 3D geometry can be derived by rotation. This structure is further called as FinFET, consisting of silicon „fin“ and its surrounding conducting gate, settled on a silicon-based substrate.

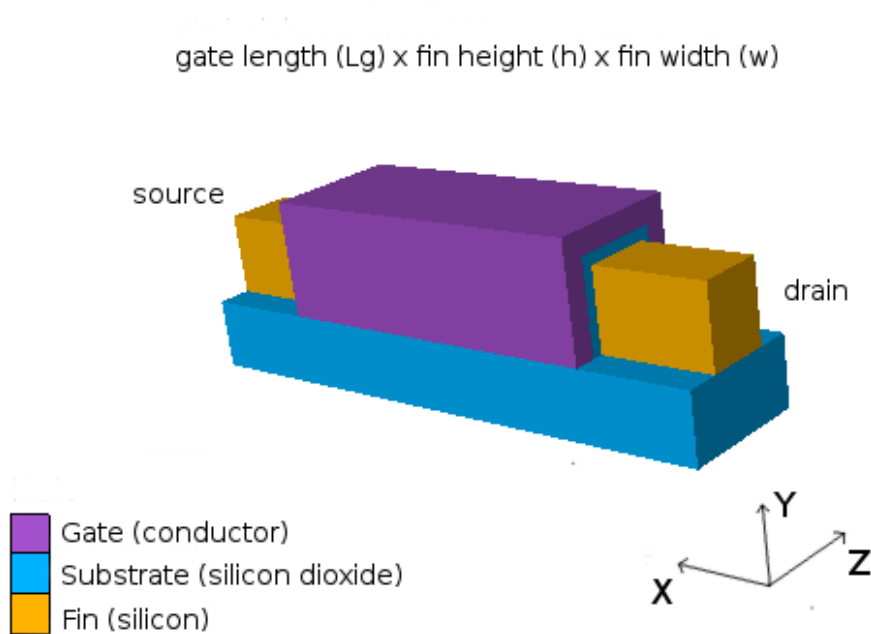
Such a FinFET structure offers more volume than a planar gate of the same planar area. Thanks to the gate geometry (Figure 1), very small current is allowed to leak through the feature when it is in the off state – so that lower threshold voltages can be applied, allowing the switching speed and power increase. According to [1], FinFET devices are prospective to be up to one third faster than planar MOSFETs and could lower its static leakage current up to 90%.

FinFET structures also promise to reduce the run time of the transistor as well, while using the same amount of power as the planar MOSFET. Together with short-channel effect subjugation, the 3D FinFET features offer an alternative for 2D devices, whose can be furthermore scaled down.

### 2 FinFET SIMULATION

In order to study the drain current and electron transmission of the FinFET device, a 3D numerical model in Silvaco TCAD software has been set up. The fin material was chosen to be silicon, the FinFET substrate was set at silicon dioxide (SiO<sub>2</sub>). The gate length (L<sub>g</sub>) of this system was scaled for L<sub>g</sub> = 1, 5, 10, 20, 30, 50, 100 and 300 nm. The fin height and fin width was held constant on values t<sub>h</sub> x w = 6 x 7 nm. The whole geometry of this device is displayed on Figure 1. The system was solved by means of drift-diffusion and quantum transport models.

## FinFET



**Fig. 1** FinFET geometry – the height, width and length of a FinFET structure is referred to its fin height and width and to its gate length, both defined in the geometry above

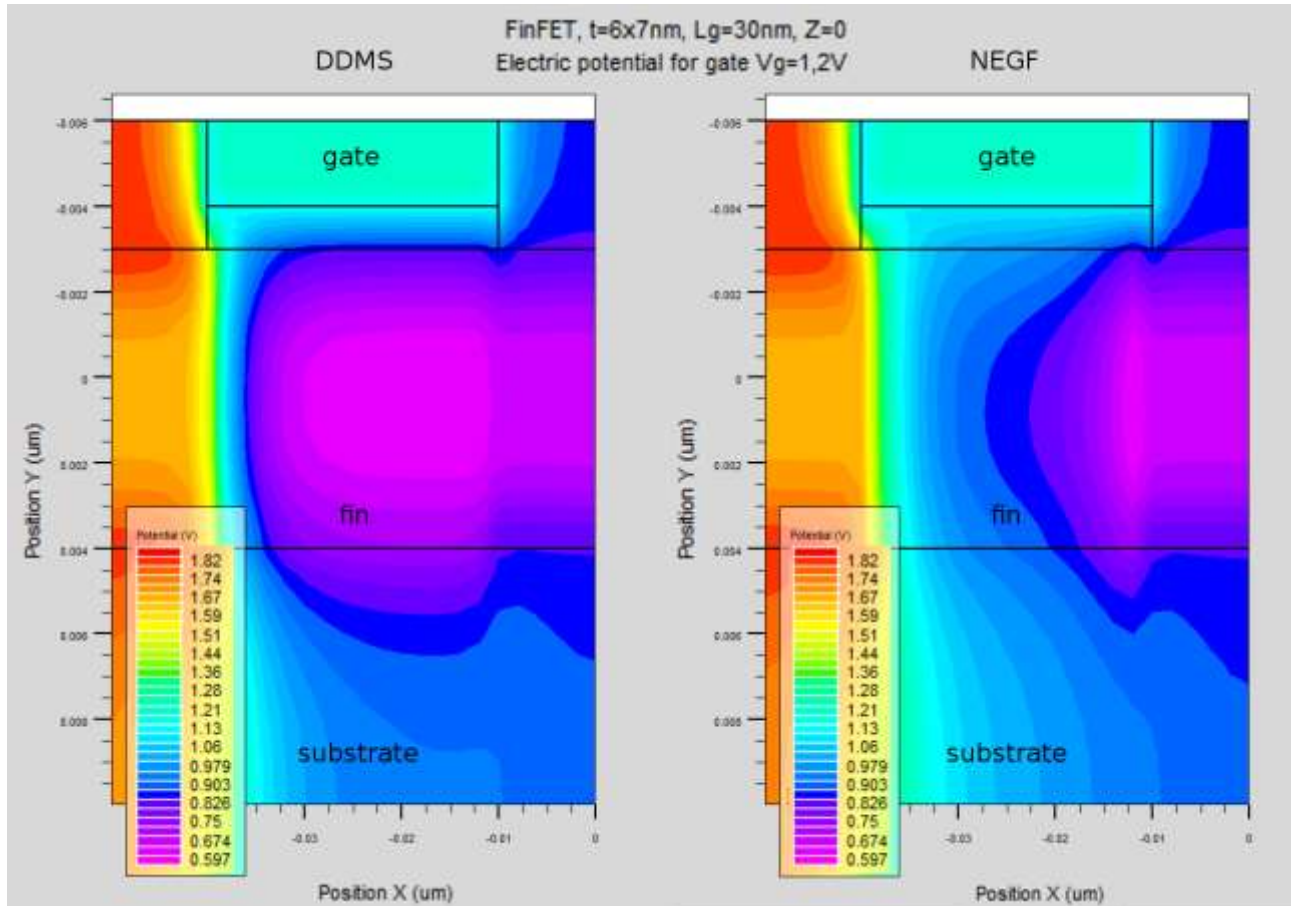
### 2.1 System setup

A FinFET model was created by means of Silvaco TCAD [3]. The geometry of the problem, as displayed on Figure 1, was meshed with in X-direction (direction of transport) 25, Y-direction 53 and in Z-direction 24 constant wide cells, excluding electrodes at the sides which were treated more roughly. For each model, left and right electrode area was dimensioned for 10 nm. Models with 7 different gate lengths (X-direction) were studied, thus the ratio of gate length and electrode length changed. The Schrödinger-Poisson (SP) mesh in X-direction was 10x finer than geometry X-direction mesh, SP meshes in Y- and Z-direction were the same as the geometry meshes. N-type charge concentration in electrodes region was set to  $10^{20} \text{ cm}^{-3}$ , electron saturation velocity to  $v_s = 1,1 \cdot 10^3 \text{ cm/s}$ . Schrodinger equation was solved by means of semi-classical approach DDMS (Drift-Diffusion Mode-Space model) and by means of quantum approach NEGF-MS (Non-Equilibrium Green's Functions Mode-Space). Similarly, using its NEGF solver, a FinFET model with this geometry was set up in the QuantumWise Atomistix ToolKit (ATK, [4]) software as well. Gate voltage was alternated between 0 and 1.2 V.

## 3 RESULTS

Drain current and electron transmission were successfully computed for gate lengths  $L = 1, 5, 10, 20, 30, 50$  and 100 nm. We tried shorter and larger gate lengths ( $L_g = 1 \text{ nm}$ ,  $L_g = 300 \text{ nm}$ ) but these dimensions touch the numerical capability of the chosen methods (especially electron transmission with NEGF method) and the TCAD simulations were not successful for these devices. Such restriction, however, doesn't limit the study because, as it will be shown later, the computation window covers the whole transition zone and at the borders of the gate length interval, no more changes in the system behavior were observed. Although the smallest geometry possible for ATK software was chosen ( $L = 3 \text{ nm}$ ), its computation was unfortunately too time-consuming and it was not possible to finish it.

A comparison of DDMS and NEGF models for FinFET device is displayed on Figure 2. The potential field (cut plane  $Z = 0$ ) for drain voltage  $V_d = 1,0$  V and gate voltage  $V_g = 1,2$  V after the computation shows differences in the middle area – according to NEGF solver, the potential isoplanes are axisymmetric around X-axis. The potential field in the fin out of gate are then very close for both solvers.

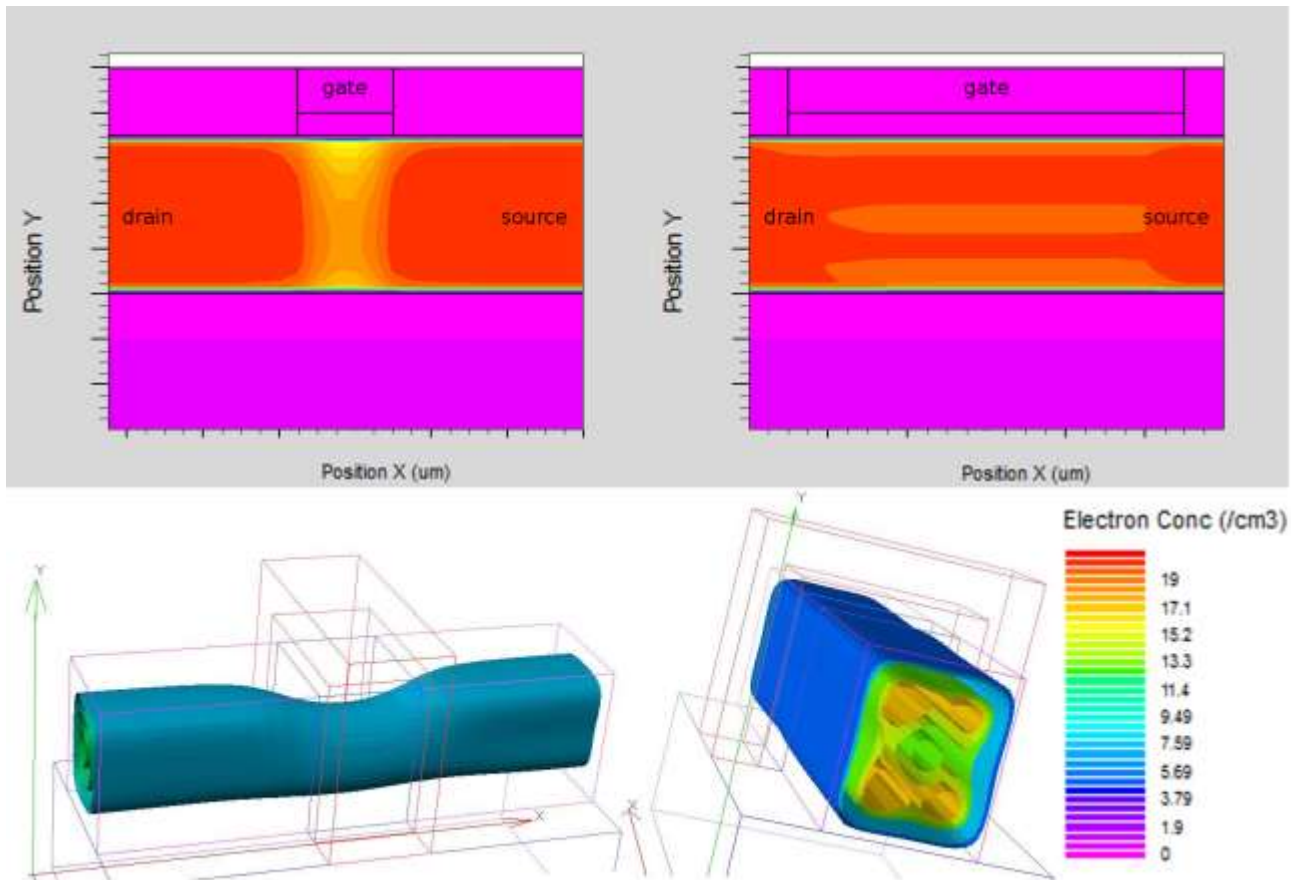


**Fig. 2** FinFET - potential on the device after the simulation using DDMS (left) and NEGF (right) solver, Silvaco TCAD: drain voltage (left border)  $V_d = 1,0$  V, gate voltage  $V_g = 1,2$  V, cut plane for  $Z = 0$

By varying the gate length, the isoplanes of ca. 0.5-0.8 V (by source on the right side, dark blue to purple) grow from just vertical planes to this parabola-like shape which length grows. It does exist a definite maximal length of this parabola which is achieved by ca.  $L_g = 50$  nm. For gate lengths  $L_g > 50$  nm, therefore, no more changes in gate voltage – drain current behavior is to be expected. The electron concentration in the FinFET device for two different gate voltages is shown on Figure 3. If the voltage on the gate is set to zero, a narrower channel appears in the volume under the gate, the electron concentration sinks. For higher gate voltages, the electron concentration tends to grow up under the gate and the whole electron channel is straighter. Local channels with higher electron density are build under the gate, especially near to the boundaries.

### 3.1 Drain current

As seen on Figure 4, the results for DDMS and NEGF computation are very similar qualitatively but quantitatively are they by more orders shifted to each other. Thus, for shape study and drain current characteristics overview, faster DDMS method can be used. But for the correct value estimation, more accurate and more time-demanding NEGF method has to be used.



**Fig. 3** Electron concentration for FinFET device, left column: zero voltage on gate ( $V_d=1,0V$ ,  $V_g=0,0V$ ), right column: full voltage on gate ( $V_d=1,0V$ ,  $V_g=1,2V$ ), NEGF solver, Silvaco TCAD

$L_g=1\text{nm}$  and  $L_g=5\text{nm}$  embodies very flat drain current characteristics – the transistor is just voltage independent and even for zero voltages on the gate in open, conducting state. Very huge differences between drain current for zero gate voltages are then obtained for  $L_g = 10\text{ nm}$  and  $L_g = 20\text{ nm}$  – over 5 orders. Thus, only when the gate length lies between 5 nm (conductor-like behavior) and 20 nm (transistor-like behavior) the gate presence start to influence the fin current. For gates longer than 20 nm, the drain current sinks for zero voltage on gate two orders maximally ( $L_g = 50\text{nm}$ ) and stay stable even for longer gates.

Therefore, a functional FinFET device with fin size  $6 \times 7\text{ nm}$  only for gates length in interval between 10 nm – 50 nm leads to transistor-like behavior with different drain current slope for gate voltages.

### 3.2 Transmission of electrons

Calculated transmission of electrons is displayed on Figure 5. Transmissions for  $L_g > 50\text{ nm}$  are not shown because the NEGF numerical method wasn't able to solve this problem appropriate.

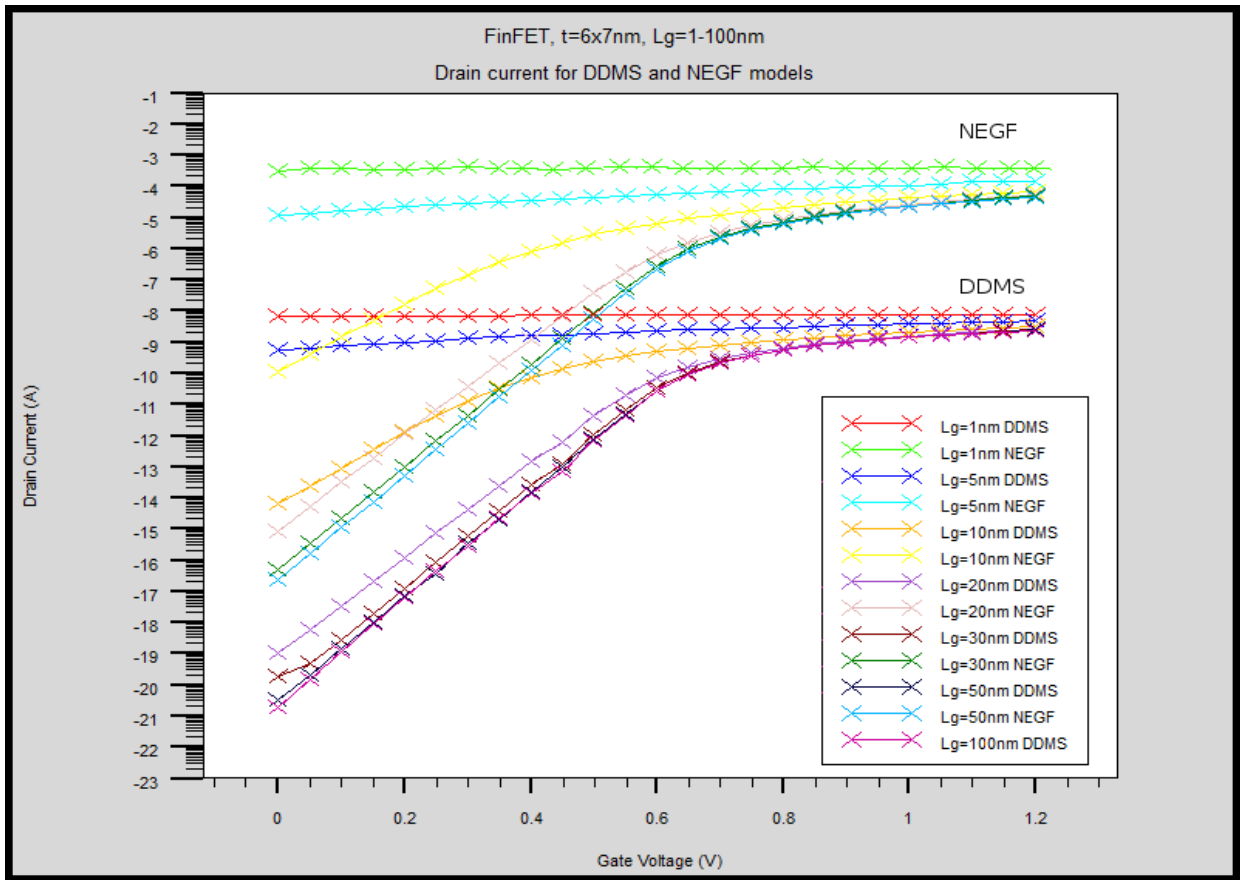


Fig. 4 Drain current computed by means of DDMS for gate lengths  $L_g = 1$  to  $100 \text{ nm}$

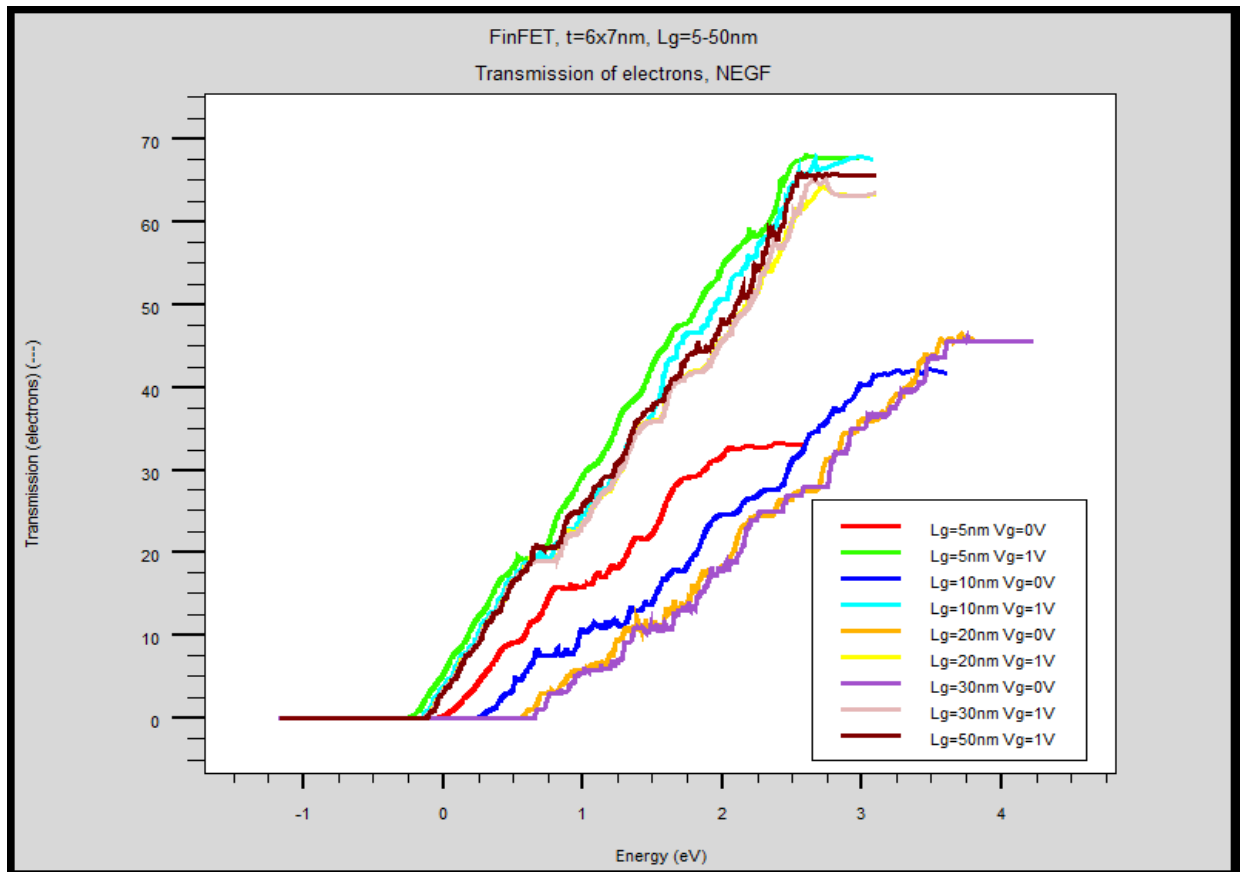


Fig. 4 Transmission of electrons for gate length  $L_g = 5$  to  $50 \text{ nm}$

As seen on the figure, the electron transmission is rather gate length independent if the gate is set to potential 1.2 V. Its slope is further steeper than for zero gate voltages. Gate length affected are the electron transmissions for zero voltage on gate. The shorter the gate is, the faster the function achieves the saturation state. For shorter gates, further, the saturation transmission is lower. But the slope of this function is rather gate length insensitive. For gate lengths over 20 nm, the electron transmission behavior doesn't change anymore with gate length increase. Thus, in correlation to the drain current characteristics, the FinFET device achieves the transistor behavior for gate lengths over 5 nm, over 20 nm the FinFET characteristics becomes stable and gate length independent.

#### 4 CONCLUSIONS

In this paper, the FinFET device characteristics – drain current and transmission of electrons – with gate length scaling was analyzed. Three-dimensional model of an FinFET transistor was simulated with Silvaco TCAD and QuantumWise ATK software. Gate length was varied between 1 and 100 nm, fin size (6 x 7 nm width and height) was held constant. It was shown, that the classical method, DDMS, can delivery accurate qualitatively data but not quantitatively; therefore, the quantum method, NEGF, is needed for accurate value estimation. According to drain current characteristics study, the FinFET device behaves for gate lengths under 10 nm rather than a conductor and only for longer gates like a transistor. For gate lengths over 20 nm, the drain current characteristics becomes stable even for longer gates. For gate lengths between 5 and 20 nm, the transistor characteristics can be therefore modified on demand. Very similar are the results for electron transmission – the function slopes are gate length independent for both gate voltages studied ( $V_g = 0.0$  V and  $V_g=1.2$ V), the electron transmission for gate voltage 1.2 V is further completely gate length independent. Electron transmission for zero gate voltage is the gate length independent only for  $L_g > 20$  nm.

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